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Novel Buck Mode Three-Level Direct AC Converter with a High Frequency Link

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Abstract

A novel family of Buck mode three-level direct ac converters with a high frequency link is proposed. These converters can transfer an unsteady high ac voltage with distortion into a regulated sinusoidal voltage with a low THD at the same frequency. The circuit configuration is constituted of a three-level converter, high frequency transformer, cycloconverter, as well as input and output filters. The topological family includes forward, push-pull, half-bridge, and full-bridge modes. In order to achieve a reliable three-level ac-ac conversion, and to overcome the surge voltage and surge current of the cycloconverter, a phase-shifted control strategy is introduced in this paper. A prototype is presented with experimental results to demonstrate that the proposed converters have five advantages including high frequency electrical isolation, lower voltage stress of the power switches, bi-directional power flow, low THD of the output voltage, and a higher input power factor.

Key words: Buck mode, Direct ac converter, High frequency link, Three-level (TL)

I. INTRODUCTION

In recent years, ac converters have become widely used in various industrial domains. However, recent research on ac converter technology has mainly focused on two-level ac converters and ac-dc-ac type multilevel ac converters [1]-[4]. The former includes ac converters with and without electrical isolation such as ac choppers, thyristor phase-controlled cycloconverters and matrix converters. The latter includes ac converters with no electrical isolation as well as those with low or middle frequency electrical isolation.

Nowadays, ac converters are required for both low-voltage input applications and high-voltage input applications. In these fields, the multilevel technique has been effectively used to reduce voltage stress with an improved output voltage quality. The multilevel technique was first proposed in dc-ac inverters [5]-[15]. Then it was developed in dc-dc converters and ac-dc rectifiers [16]-[20]. So far, the multilevel technique used in ac converters has been mainly limited to ac-dc-ac type ac converters. These converters usually have many shortcomings such as too many power conversion stages, unidirectional power flow, low input power factor, and weak adaptability to various loads. Several multilevel direct ac converters were proposed in [21]-[25]. These converters have advantages such as a single power conversion stage (LFAC-LFAC), bi-directional power flow, higher input power factor, lower voltage stress of the power switches, and strong adaptability to various loads. However, they all have no electrical isolation. Therefore, a novel high frequency isolated half-bridge three-level AC/AC converter was proposed to improve multilevel direct ac converters [26].

A novel family of Buck mode three-level direct ac converters with a high frequency link is proposed in this paper. In order to achieve reliable three-level ac-ac conversion, a strategy for phase-shifted control is also presented. The converters proposed in this paper have two-stage power conversion (LFAC-HFAC-LFAC), a bi-directional power flow, and a higher input power factor when compared with ac-dc-ac type TL ac converters. These converters have lower voltage stress of the power switches when compared with two-level ac converters. In addition, they have a more compact structure when compared with those with low or middle frequency electrical isolation. However, their efficiency is influenced by high switching device counts. These converters are targeted to be used on a new type of regulated sinusoidal ac power supply, electronic transformers and ac regulators, where high-voltage input and high frequency

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electrical isolation and/or bidirectional power flows are needed.

II. PROPOSED TOPOLOGIES

The circuit topological family of Buck mode three-level direct ac converters with a high frequency link is proposed, as shown in Fig. 1. All of the proposed converters have the same circuit configuration, which is constituted of a three-level converter, high frequency transformer, cycloconverter as well as input and output filters. The converters can transfer unsteady high ac voltage with distortion into regulated sinusoidal voltage with a low THD at the same frequency. The topological family includes the forward mode, interleaving forward mode, push-pull full-wave mode, push-pull full-bridge mode, half-bridge full-wave mode, half-bridge full-bridge mode, full-bridge full-wave mode and full-bridge full-bridge mode. These converters have advantages such as high-frequency electrical isolation, two-power conversion (LFAC-HFAC-LFAC), a bi-directional power flow, a higher input power factor, strong ability to differentiate loads, lower voltage across power switches, and soft commutation of the cycloconverter.

A comparison of the proposed topologies is shown in Table I. From Table I, it can be seen that the voltage stress for all of the topologies can be lowered more than that of two-level ac converters. It can also be seen that the full-bridge full-bridge mode topology is better suited for a larger power output.

III. CONTROL STRATEGY AND STEADY PRINCIPLE

The phase-shifted control strategy of the proposed converters is presented. Taking the push-pull full-wave mode circuit topology shown in Fig. 1(c) as an example, S_{1a} and S_{4a} are the leading-arm power switches, and S_{2a} and S_{3a} are the lagging-arm power switches. There is a phase difference θ of ($0\sim180^{o}$) between the leading-arm and the lagging-arm of the three-level converter. In addition, the voltage across the output filter u_{AB} is a uni-polarity SPWM voltage. The output voltage u_o can be adjusted and kept stable by adjusting θ sinusoidally when the input voltage u_i or the load R_L varies.

By using phase-shifted control between the leading-arm and the lagging-arm of a three-level converter, a three-level voltage across the high frequency transformer can be achieved, and the cycloconverter can commutate when the bi-polar three-level high frequency ac voltage from the three-level converter is zero. Therefore, the voltage across the power switches of the three-level converter is lowered, and the current of the output filter inductor is naturally commutated. The ZVS of the cycloconverter can be realized, and the surge voltage and surge current of the cycloconverter are overcome.

Before analyzing the steady principle, the following assumptions are made: (1) the inductors, capacitors, and resistors are ideal devices; (2) the power switches are ideal control devices; (3) the delay time of the switching is neglected. Principal waveforms within one switching period T_s ($t_1\sim t_{13}$) are shown in Fig. 2 (the control strategy of the negative half cycle is the same as that of the positive half cycle). From Fig. 2, it can be seen that the flux in the high frequency transformer is balanced over each switching period. During one T_s, there are twelve switching modes in the CCM shown in Fig. 3.

Another switching cycle starts at t_{13}. Therefore, there is a total of three levels (u_i, 0, $-u_i$) in the voltage across the high frequency transformer, and the power switches of the cycloconverter can realize ZVS soft commutation.

Fig. 4 shows equivalent circuits of the twelve switching modes during one T_s, where r includes the equivalent resistance of the high frequency transformer, the on resistance of the power switches, the parasitic resistance of the filter inductor and so on.

Since the switching frequency f_s is sufficiently higher than both the cut-off frequency f_c of the L_f-C_f filter and the modulation frequency f_o (i.e. the frequency of u_i and u_o), the state-space averaging method can be used to establish the equations of i_{Lf}, u_o and u_i. By using this, the output characteristic in the actual state ($r \neq 0$) and the CCM is given by:

$$I_{Lf}=\frac{DU_iN_3}{N_1}\frac{1}{R_L+r} \tag{1}$$

$$U_o=\frac{DU_iN_3}{N_1}\frac{1}{1+r/R_L} \tag{2}$$

In (1) and (2), D is the duty cycle of the SPWM voltage u_{AB} across the output filters during one T_s. From (2), the output characteristic in the ideal state (r=0) and the CCM is given by:

$$U_o = DU_iN_3/N_1 \tag{3}$$

Similarly, the output characteristic in the ideal state (r=0) and the critically CCM is given by:

$$I_o = 4I_{G\max}D(1-D) \tag{4}$$

The output characteristic in the ideal state (r=0) and the DCM is given by:

$$\frac{U_o}{U_i}=\frac{4D^2}{4D^2+I_o/I_{G\max}}\frac{N_3}{N_1} \tag{5}$$

In (4) and (5), I_o is the load current, I_{Gmax} is the maximum value of I_o in the critically CCM and $I_{Gmax}=U_iN_3T_s/(16N_1L_f)$.

IV. DESIGN CONSIDERATIONS

The design specifications of the push-pull mode TL ac direct converter are defined as follows: input voltage U_i=198-242V(50Hz) ac, output voltage U_o=110V(50Hz) ac,

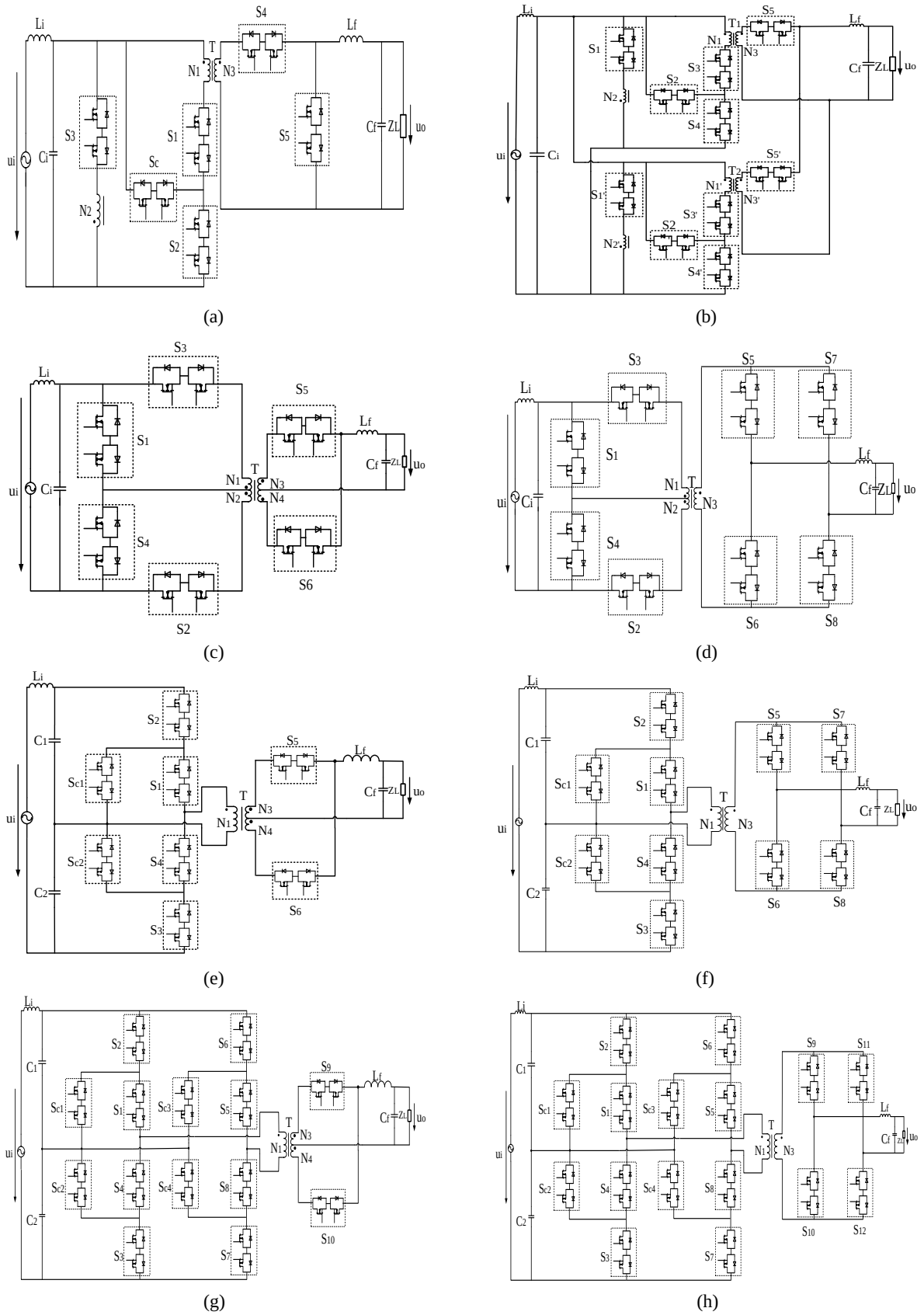


Fig. 1. Circuit diagrams for the proposed topological family. (a) Forward mode. (b) Interleaving forward mode. (c) Push-pull full-wave mode. (d) Push-pull full-bridge mode. (e) Half-bridge full-wave mode. (f) Half-bridge full-bridge mode. (g) Full-bridge full-wave mode. (h) Full-bridge full-bridge mode.

TABLE I
COMPARISON OF THE PROPOSED TOPOLOGIES

performances / topologies	active components count	passive components count	voltage stresses of three-level converter	voltage stresses of cycloconverter	voltage gain
forward mode	12	4	$\left(1+\frac{N_2}{N_1}\right)\sqrt{2}U_{i\max}$	$\frac{N_3}{N_1}\sqrt{2}U_{i\max}$	$\frac{DN_3}{N_1}\frac{R_L}{r+R_L}$
interleaving forward mode	20	4	$\left(1+\frac{N_2}{N_1}\right)\sqrt{2}U_{i\max}$	$\frac{N_3}{N_1}\sqrt{2}U_{i\max}$	$\frac{2DN_3}{N_1}\frac{R_L}{r+R_L}$
push-pull full-wave mode	12	4	$\sqrt{2}U_{i\max}$	$\frac{N_3}{N_1}2\sqrt{2}U_{i\max}$	$\frac{DN_3}{N_1}\frac{R_L}{r+R_L}$
push-pull full-bridge mode	16	4	$\sqrt{2}U_{i\max}$	$\frac{N_3}{N_1}\sqrt{2}U_{i\max}$	$\frac{DN_3}{N_1}\frac{R_L}{r+R_L}$
half-bridge full-wave mode	16	5	$\frac{\sqrt{2}U_{i\max}}{2}$	$\frac{N_3}{N_1}\sqrt{2}U_{i\max}$	$\frac{DN_3}{2N_1}\frac{R_L}{r+R_L}$
half-bridge full-bridge mode	20	5	$\frac{\sqrt{2}U_{i\max}}{2}$	$\frac{N_3}{N_1}\frac{\sqrt{2}}{2}U_{i\max}$	$\frac{DN_3}{2N_1}\frac{R_L}{r+R_L}$
full-bridge full-wave mode	28	5	$\frac{\sqrt{2}U_{i\max}}{2}$	$\frac{N_3}{N_1}\sqrt{2}U_{i\max}$	$\frac{N_3}{N_1}\frac{1+D_1-D_2}{2}\frac{R_L}{r+R_L}$
full-bridge full-bridge mode	32	5	$\frac{\sqrt{2}U_{i\max}}{2}$	$\frac{N_3}{N_1}\frac{\sqrt{2}}{2}U_{i\max}$	$\frac{N_3}{N_1}\frac{1+D_1-D_2}{2}\frac{R_L}{r+R_L}$

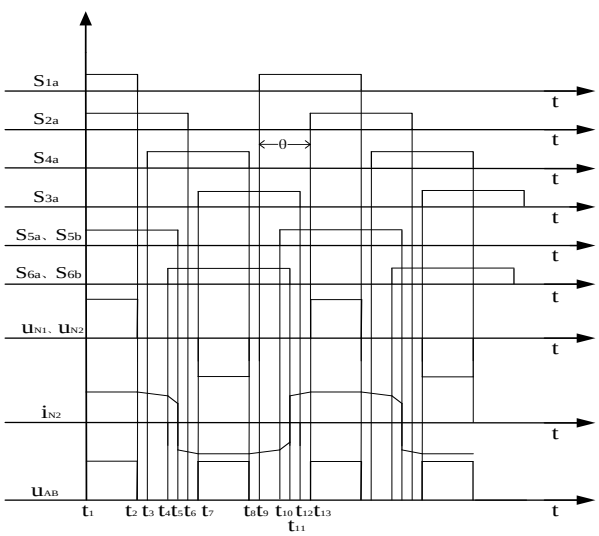


Fig. 2. Principal waveforms within one switching period T_s.

$t=t_1$-t_2: The power switch S_{2a} is turned on with the voltage u_i at t_1; the current of the primary windings of the high frequency transformer i_{N1} begins to flow through S_{1a}, $S_{1b}(D_{1b})$, S_{2a}, S_{2b} (D_{2b}), and the voltage across the primary winding $u_{N2}=u_i$; the current of the output filter inductor i_{Lf} flows through S_{5a}, $S_{5b}(D_{5b})$, and the voltage across the output filters $u_{AB}=u_iN_3/N_2$.

$t=t_2$-t_3: S_{1a} is turned off with ZVS at t_2; the voltage across S_{1a} increases quickly from 0 to u_i, and the voltage across S_{4a} decreases quickly from u_i to 0; i_{N1} begins to flow through S_{4b}, D_{4a}, S_{2a}, S_{2b} (D_{2b}), and $u_{N2}=0$; i_{Lf} begins to flow through S_{5a}, $S_{5b}(D_{5b})$, and $u_{AB}=0$.

$t=t_3$-t_4: S_{4a} is turned on with ZVS at t_3; i_{N1} flows through S_{4b}, $S_{4a}(D_{4a})$, S_{2a}, $S_{2b}(D_{2b})$, and $u_{N2}=0$; i_{Lf} flows through S_{5a}, $S_{5b}(D_{5b})$, and $u_{AB}=0$.

$t=t_4$-t_5: S_{6a} and S_{6b} are turned on with ZVS at t_4; i_{N1} still flows through S_{4b}, $S_{4a}(D_{4a})$, S_{2a}, $S_{2b}(D_{2b})$, and $u_{N2}=0$; i_{Lf} flows through S_{5a}, $S_{5b}(D_{5b})$, and $u_{AB}=0$. This time interval is the commutation overlap time of the cycloconverter to guarantee the continuity of i_{Lf}.

$t=t_5$-t_6: S_{5a} and S_{5b} are turned off with ZVS at t_5; i_{N1} flows through S_{2b}, $S_{2a}(D_{2a})$, S_{4a}, $S_{4b}(D_{4b})$, and $u_{N2}=0$; i_{Lf} flows through S_{6a}, $S_{6b}(D_{6b})$, and $u_{AB}=0$.

$t=t_6$-t_7: S_{2a} is turned off with ZVS at t_6; i_{N1} flows through S_{4a}, $S_{4b}(D_{4b})$, S_{2b}, D_{2a}, and $u_{N2}=0$; i_{Lf} flows through S_{6a}, $S_{6b}(D_{6b})$, and $u_{AB}=0$.

$t=t_7$-t_8: S_{3a} is turned on with the voltage u_i at t_7; i_{N1} flows through S_{3a}, $S_{3b}(D_{3b})$, S_{4a}, $S_{4b}(D_{4b})$, and $u_{N1}=-u_i$; i_{Lf} still flows through S_{6a}, $S_{6b}(D_{6b})$, and $u_{AB}=u_iN_4/N_1$.

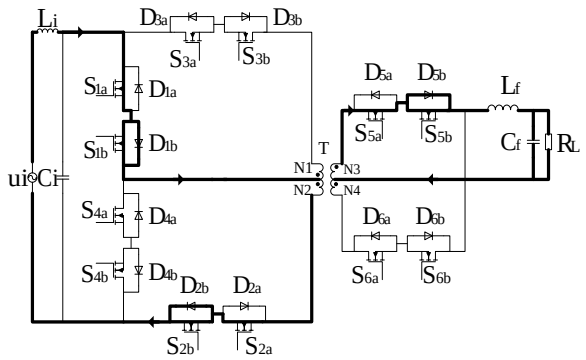
$t=t_8$-t_9: S_{4a} is turned off with ZVS at t_8; the voltage across S_{4a} increases quickly from 0 to u_i; i_{N1} begins to flow through S_{3a}, $S_{3b}(D_{3b})$, S_{1b}, D_{1a}, and $u_{N1}=0$; i_{Lf} begins to flow through S_{6a}, $S_{6b}(D_{6b})$, and $u_{AB}=0$.

$t=t_9$-t_{10}: S_{1a} is turned on with ZVS at t_9; i_{N1} flows through S_{3a}, $S_{3b}(D_{3b})$, S_{1b}, $S_{1a}(D_{1a})$, and $u_{N1}=0$; i_{Lf} flows through S_{6a}, $S_{6b}(D_{6b})$, and $u_{AB}=0$.

$t=t_{10}$-t_{11}: S_{5a} and S_{5b} is turned on with ZVS at t_{10}; i_{N1} still flows through S_{3a}, $S_{3b}(D_{3b})$, S_{1b}, $S_{1a}(D_{1a})$, and $u_{N1}=0$; i_{Lf} flows through S_{6a}, $S_{6b}(D_{6b})$, and $u_{AB}=0$. This time interval is the commutation overlap time of the cycloconverter.

$t=t_{11}$-t_{12}: S_{6a} and S_{6b} is turned off with ZVS at t_{11}; i_{N1} flows through S_{1a}, $S_{1b}(D_{1b})$, S_{3b}, $S_{3a}(D_{3a})$, and $u_{N1}=0$; i_{Lf} flows through S_{5a}, $S_{5b}(D_{5b})$, and $u_{AB}=0$.

$t=t_{12}$-t_{13}: S_{3a} is turned off with ZVS at t_{12}; i_{N1} flows through S_{1a}, $S_{1b}(D_{1b})$, S_{3b}, D_{3a}, and $u_{N1}=0$; i_{Lf} flows through S_{5a}, $S_{5b}(D_{5b})$, and $u_{AB}=0$.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D5a
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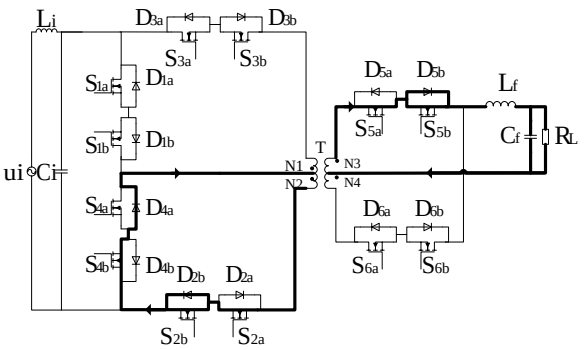
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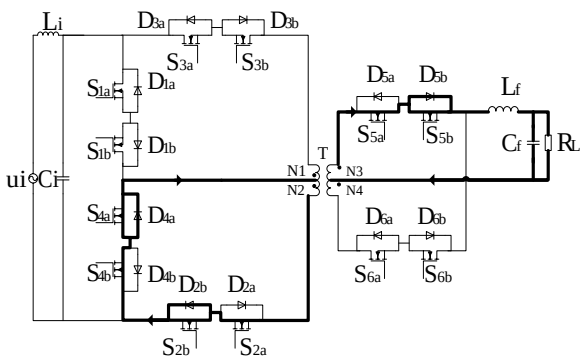
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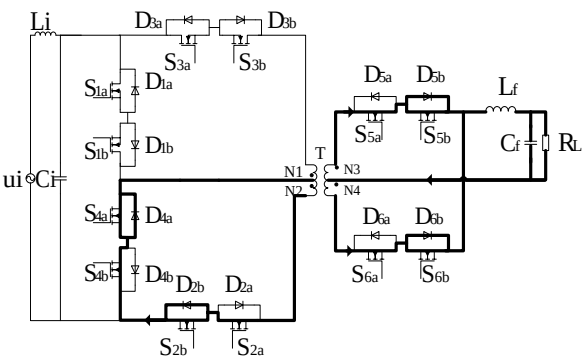
Li
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D4b
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N4
D5a
D5b
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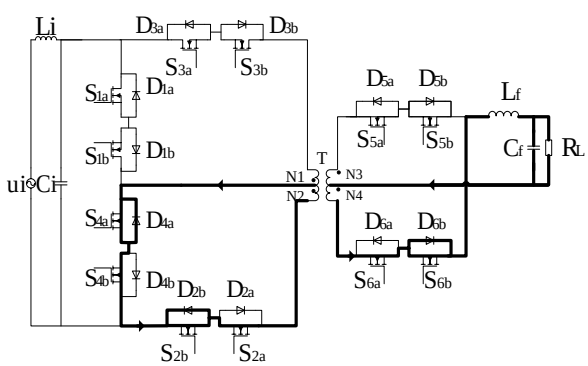
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N4
D5a
D5b
Lf
S5a
S5b
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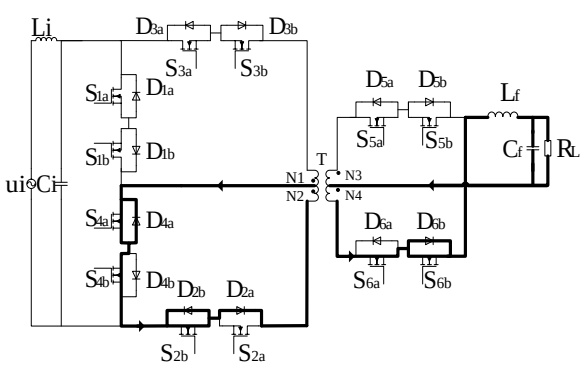
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N4
D5a
D5b
Lf
S5a
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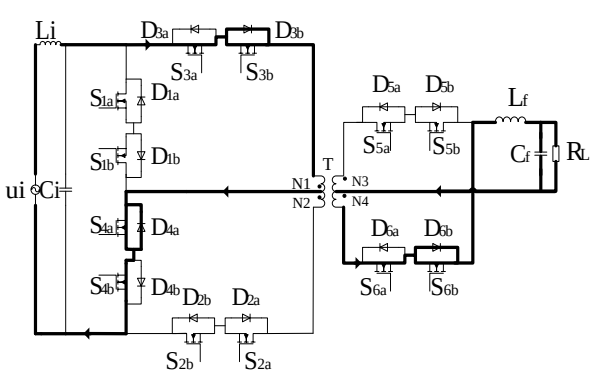
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D4b
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D5a
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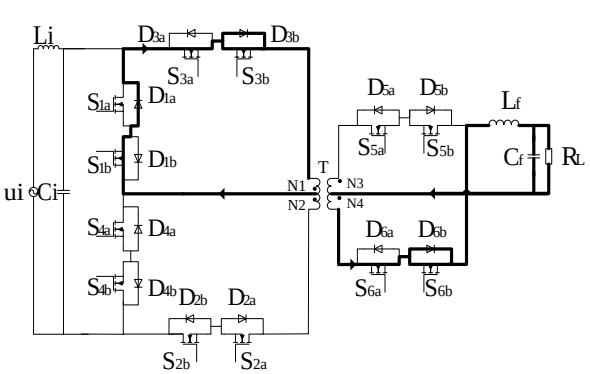
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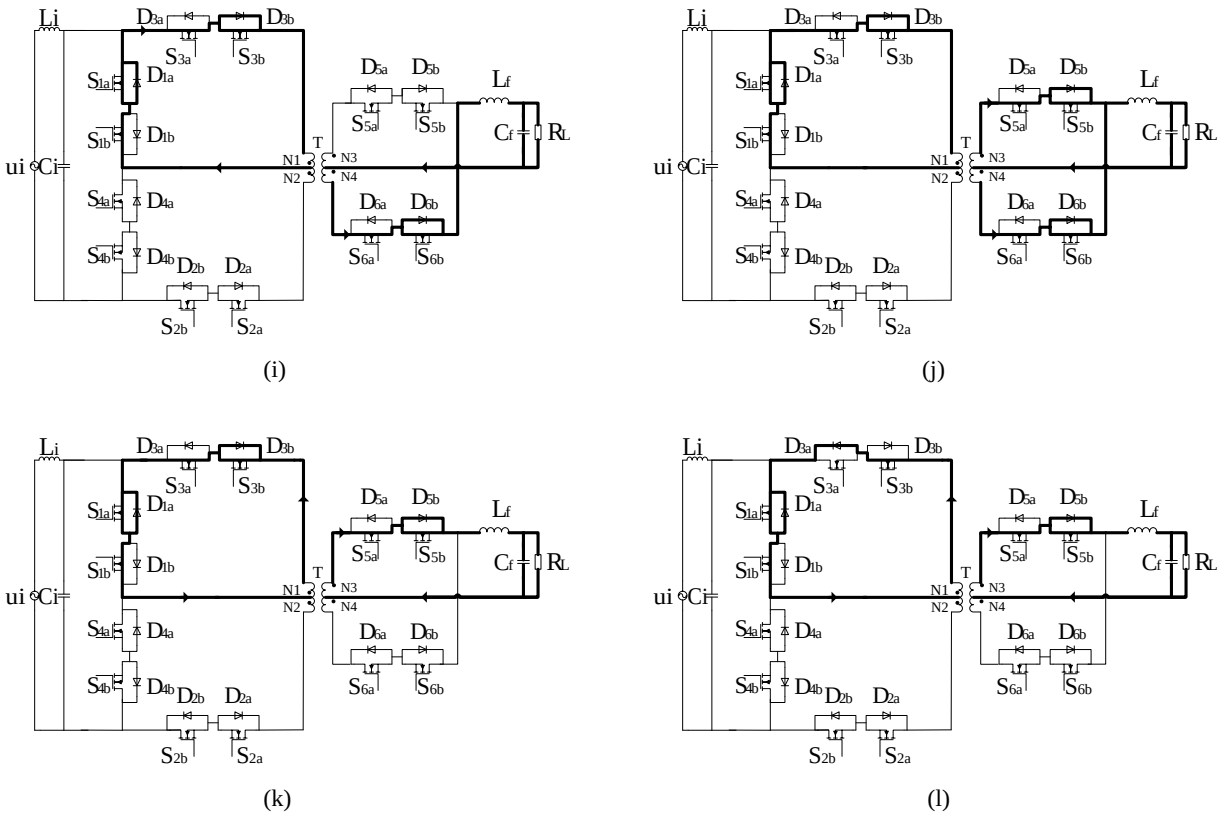


Fig. 3. Twelve switching modes in the CCM during one switching period T_s. (a) [t1- t2]. (b) [t2- t3]. (c) [t3- t4]. (d) [t4- t5]. (e) [t5- t6]. (f) [t6- t7]. (g) [t7- t8]. (h) [t8- t9]. (i) [t9- t10]. (j) [t10- t11]. (k) [t11- t12]. (l) [t12- t13].

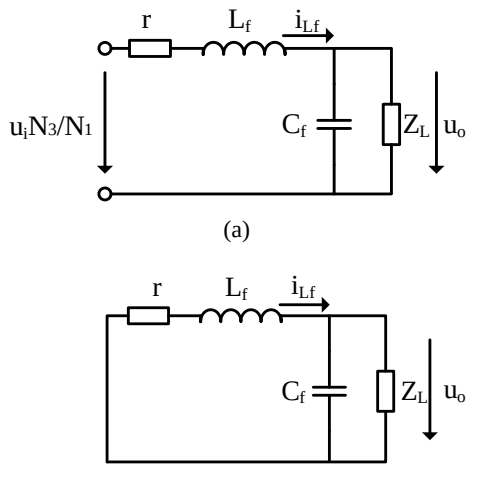


Fig. 4. Equivalent circuits in the CCM during one T_s. (a) State 1. (b) State 2.

normalized capacity S=500VA, maximum duty cycle D_{max}=0.8, pulsating current of $i_{Lf} \Delta i_{Lf} \leq 0.1\times\sqrt{2}I_{o,max}$, current of the output filter capacitor $i_{Cf} \leq 0.05I_{o,max}$, and equivalent resistance of the converter r=0.5Ω.

To ensure the operation of the converter, the circuit parameters including f_s, the high frequency transformer, C_f, L_f and S_{1a}~S_{6b} are determined as follows.

A. Determining the Switching Frequency f_s

The higher the switching frequency f_s is, the less the filters will be at a cost of more switching losses. Therefore, f_s is chosen to be 50kHz as a trade-off.

B. Determining the High Frequency Transformer

From (2), the turn ratio of the high frequency transformer N_3/N_1 is given by:

$$\frac{N_3}{N_1}=\frac{\sqrt{2}U_{o,\max}}{\sqrt{2}U_{i,\min}D_{\max}}\left(1+\frac{r}{R_{L,\min}}\right)$$

$$=\frac{\sqrt{2}\times 110}{\sqrt{2}\times 198\quad 0.8}\times\left(1+\frac{0.5}{24.2}\right)=0.\quad (6)$$

Some losses including conduction losses and switching losses of the power switches are considered. Therefore, N_3/N_1 is selected as 0.7.

A LP3 PM74 core with a 5100Gs saturated flux is selected for the transformer, whose effective magnetic circuit area is $S=6.37cm^2$. For its operating flux density $\Delta B=2B_m=2400G_S$, the turns of the high frequency transformer's primary windings are given by:

$$N_1=N_2=\frac{\sqrt{2}U_{i,\min}T_{on,\max}}{\Delta B\cdot S}\times 10^8$$

$$= \frac{\sqrt{2}\times 198\times 0.4/(50\times 10^3)}{2400\times 6.37}\times 10^8 = 14.65 \qquad (7)$$

Then, N_1 and N_2 are chosen to be 15.

From (6) and (7), the turns of the high frequency transformer's secondary windings N_3 and N_4 are chosen to be 11. Therefore, $N_1/N_2/N_3/N_4$=15/15/11/11.

C. Determining the Output Filter Capacitance C_f

With the value of C_f increasing, the THD of the output voltage u_o decreases. However, the reactive component of the output current and the loss of the converter increase. When limited to $i_{Cf} \le 0.05 I_{o,max}$, C_f is determined by:

$$C_f \le \frac{5\%P_{o,\max}}{U_o^2\cdot 2\pi f_o} = \frac{5\%\times 500}{110^2\times 2\pi\times 50} = 6.58(\mu F) \qquad (8)$$

The maximum voltage across C_f is $\sqrt{2}U_{o,\max} = \sqrt{2}\times 110 = 156$ (V). Therefore, C_f is chosen as 4.7μF/450V.

D. Determining the Output Filter Inductance L_f

With the value of L_f increasing, the THD of the output voltage u_o decreases. However, the dynamic response of the system becomes slow. Limited to $\Delta i_{Lf} \le 0.1\times\sqrt{2}I_{o,\max}$, L_f must satisfy:

$$L_f \ge \frac{\sqrt{2}U_{i,\min}\ N_3/N_1 - \sqrt{2}U_o}{\Delta i_{Lf}}\cdot T_{on\cdot\max}$$

$$= \frac{198\sqrt{2}\times 11/15 - 110\sqrt{2}}{0.1\times\sqrt{2}\times 500/110}\cdot\frac{0.4}{50\times 10^3} = 620(\mu H) \qquad (9)$$

Then L_f is selected to be 650μH. An LP3 PM62 core is selected to be the output filter inductor, whose effective magnetic circuit area is S=4.9cm^2. For its operating flux density B_m=3300Gs, the turns of the output filter inductor is given by:

$$N = \frac{L_f I_{Lf,peak}}{B_m S}\times 10^8$$

$$= \frac{L_f\times 110\%\times\sqrt{2}\sqrt{(\omega C_f U_o)^2 + (P_{o,\max}/U_o)^2}}{B_m S}\times 10^8$$

$$= \frac{0.65\times 10^{-3}\times 7.1}{3300\times 4.9}\times 10^8 = 28.5 \qquad (10)$$

N is selected to be 29 turns. The air gap of the magnetic core is given by:

$$\delta = \mu_o N^2 S/L_f = \frac{4\pi\times 10^{-7}\times 29^2\times 4.9\times 10^{-4}}{0.65\times 10^{-3}} = 0.8(mm) \qquad (11)$$

E. Determining the Power Switches

Based on the steady principle, the maximum voltage across the power switches of the three-level converter is $\sqrt{2}U_{i,\max} = \sqrt{2}\times 242 = 342(V)$, which is only half that of two-level push-pull converters. The rms current of the power switches of the three-level converter is:

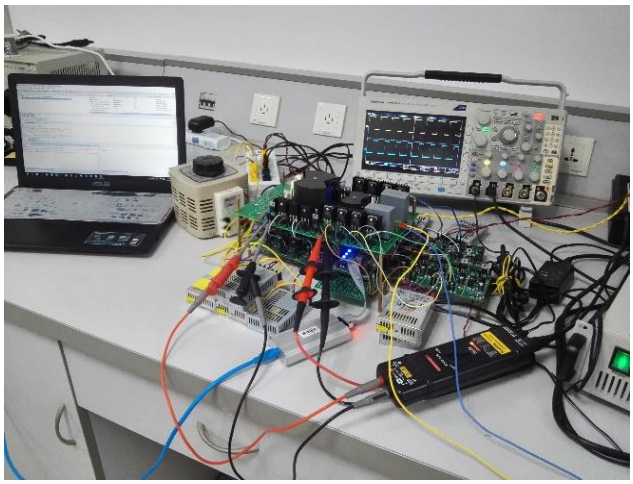


Fig. 5. Designed and developed prototype.

$$I_1 = I_{Lf}\frac{N_3}{N_1}\times 105\%$$

$$= \sqrt{(\omega C_f U_o)^2 + (P_{o,\max}/U_o)^2}\ \frac{N_3}{N_1}\times 105\%$$

$$= 4.56\times 11/15\times 105\% = 3.51(A) \qquad (12)$$

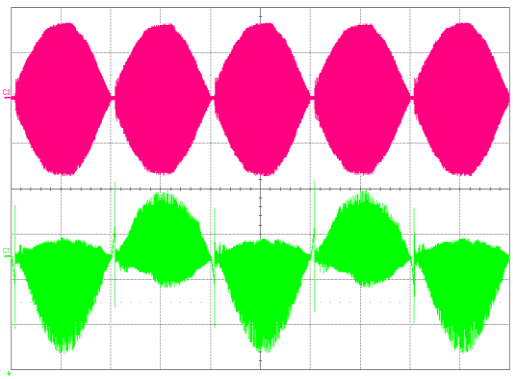
Then, MOSFETs IRFP460 (500V/20A) are chosen for the power switches S_{1a}~S_{4b}.

The maximum voltage across the power switches of the cycloconverter is $2\times\sqrt{2}U_{i,\max}\ N_3/N_1 = 2\times\sqrt{2}\times 242\times 11/15 = 502(V)$. The rms current of the power switches of the cycloconverter is $I_2 = I_{Lf}/\sqrt{2} = 3.23(A)$. Then, fast IGBTs FGA20N120FTD (1200V/20A) are chosen for the power switches S_{5a}~S_{6b}.

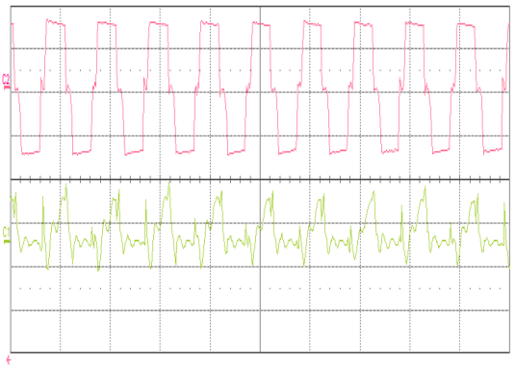
V. Prototype

The designed and developed prototype shown in Fig. 5 is as follows: push-pull mode circuit topology, phase-shifted control strategy, normalized capacity S=500VA, input voltage U_i=220V±10%(50Hz) ac, output voltage U_o=110V (50Hz) ac, switching frequency f_s=50kHz, LP3 PM74 magnetic core for the high frequency transformer, turn ratio $N_1/N_2/N_3/N_4$=15/15/11/11, output filter inductance L_f=650μH, output filter capacitance C_f=4.7μF/450V, MOSFETs (IRFP460) for S_{1a}~S_{4b}, fast IGBTs (FGA20N120FTD) for S_{5a}~S_{6b}, and load power factor $\cos\varphi_L$= -0.75~+0.75.

The developed prototype has good comprehensive performances: the normalized capacity S=500VA, U_i=198~242V(50Hz) ac, the load power factor range $\cos\varphi_L$ = -0.75~0.75, U_o=110 ± 1V, f_o=50Hz, the output voltage THD<3.5%, the conversion efficiency at the normalized different nature load is more than 80.0~87.0%, the line power factor at the normalized different nature load is more than 0.670~0.998, the DC component of u_o is less than 0.1V, and the operational time is 120 min at a 110% normalized load.



(a)



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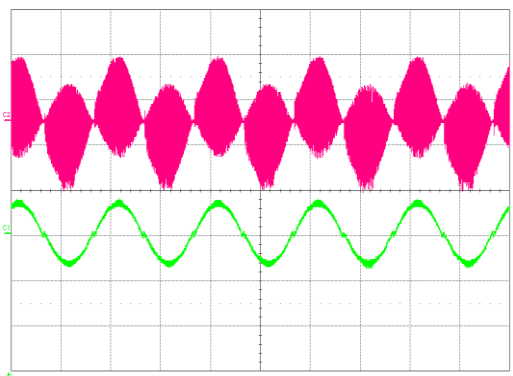
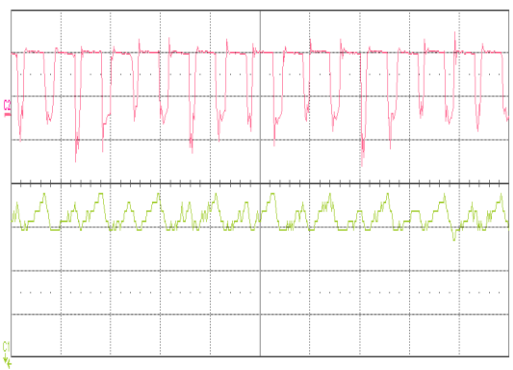
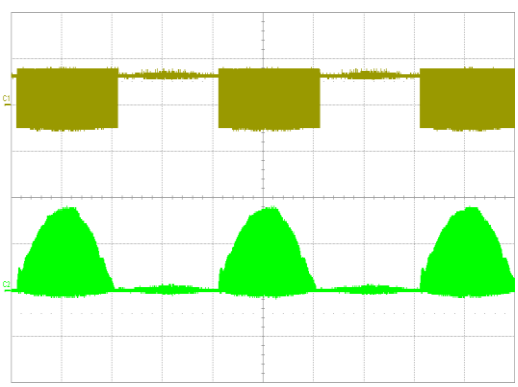


(c)



(d)



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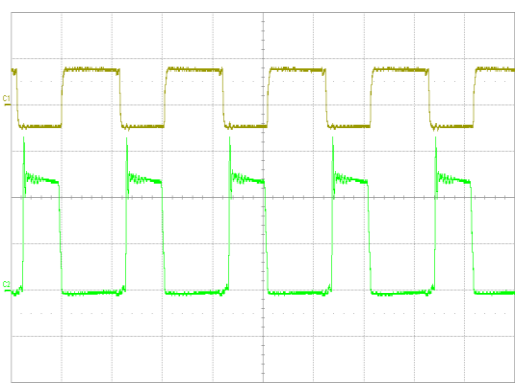
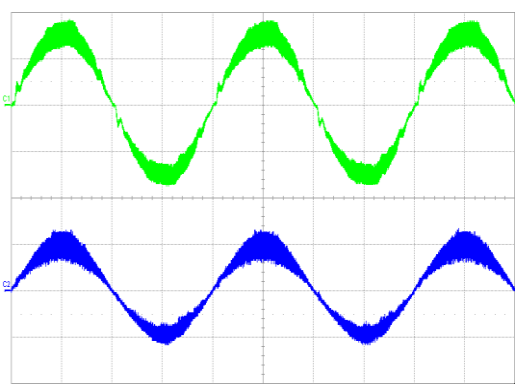
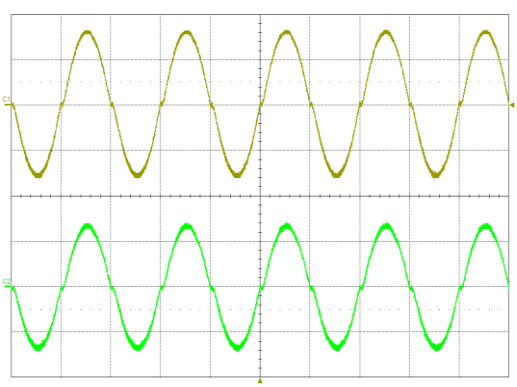


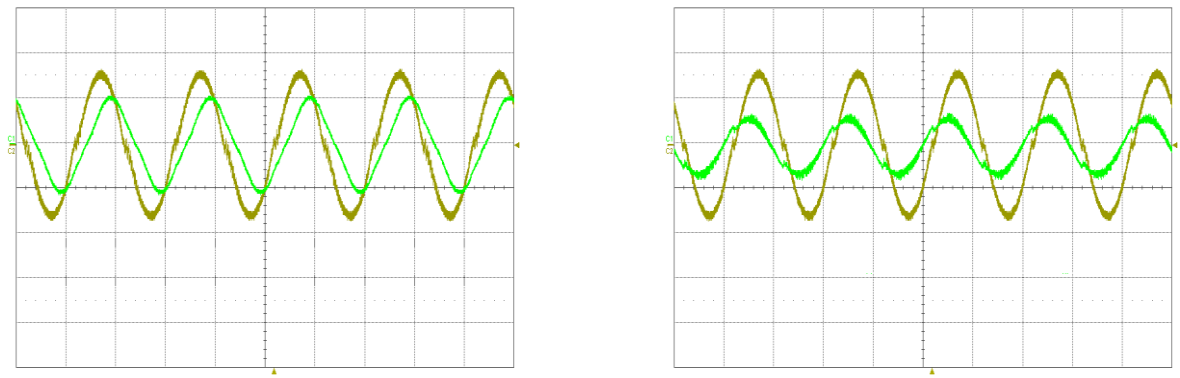
(f)



(g)

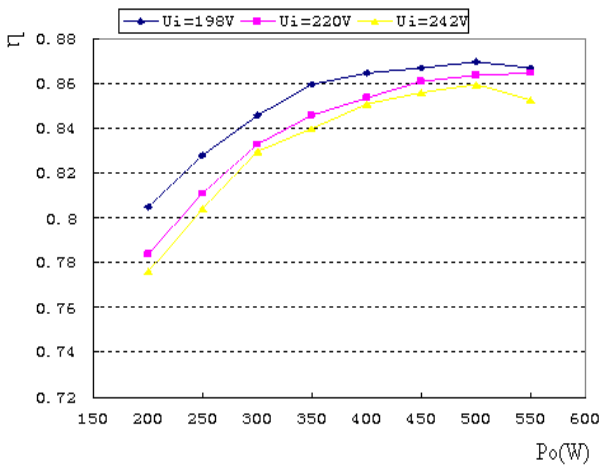


(h)

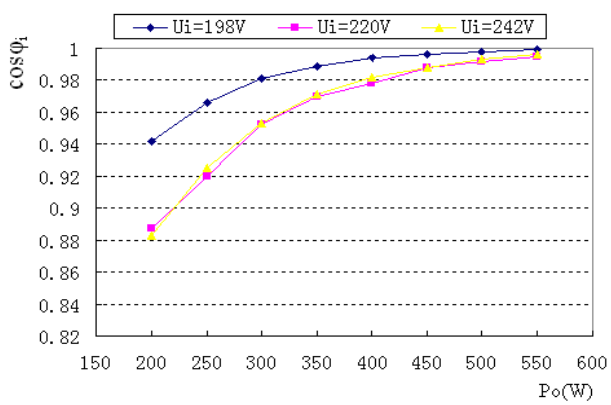


(i) (j)

Fig. 6. Principle test waveforms of the proposed converter. (a) CH2: uN1 (200V/div); CH1: iN1 (10A/div); t(5ms/div). (b) CH2: uN1 (196V/div); CH1: iN1 (9.8A/div); t(20μs/div). (c) CH2: uAB (200V/div); CH1: iLf (10A/div); t(10ms/div). (d) CH2: uAB (146V/div); CH1: iLf (1.46A/div); t(18μs/div). (e) CH1: trigger voltage ugs1a of the power switch S1a (20V/div); CH2: voltage uds1a across S1a (200V/div); t(5ms/div). (f) CH1: trigger voltage ugs5b of the power switch S5b(20V/div); CH2: voltage uds5b across S5b (200V/div); t(10μs/div). (g) CH1: input voltage ui (200V/div); CH2: reference voltage uref (5V/div); t(5ms/div). (h) CH1: uo at a resistive load (100V/div); CH2: io at a resistive load (5A/div); t(10ms/div). (i) CH1: io at a RL load (5A/div); CH2: uo at a RL load (100V/div); t(10ms/div). (j) CH1: io at a RC load (2A/div); CH2: uo at a RC load (100V/div); t(10ms/div).



(a)



(b)

Fig. 7. Conversion efficiency and line power factor versus the load at different input voltages. (a) Conversion efficiency η versus output power P_o at different input voltages u_i. (b) Line power factor $\cos\varphi_i$ versus output power P_o at different input voltages u_i.

Experimental waveforms of the proposed converter are shown in Fig. 6. As shown in Fig. 6(a) and Fig. 6(b), the voltage across the transformer u_{N1} is a bi-polarity three-level (u_i, 0, $-u_i$) high frequency voltage, and the flux in the high frequency transformer can be balanced over each high frequency switching cycle. From Fig. 6(c) and Fig. 6(d), it can be seen that the voltage across the output filter u_{AB} is a uni-polarity SPWM voltage. Fig. 6(e) shows that the voltage across the three-level converter is the input voltage, which is only half that of the push-pull mode two-level ac converter. From Fig. 6(f), it can be seen that the power switches of the cycloconverter can realize ZVS. Fig. 6(g), Fig. 6(h), Fig. 6(i) and Fig. 6(j) show that the output voltage u_o has a much lower THD than the input voltage u_i, and that the converter has strong adaptability to various kinds of loads.

Curves where the conversion efficiency and the line power factor vary with the load at different input voltages are shown in Fig. 7. From Fig. 7, it can be seen that the converter has a higher conversion efficiency and a line power factor. With the output power increasing, both the conversion efficiency and the line power factor of the converter increase, and they reach their maximum value at the nearest normalized capacity.

VI. CONCLUSIONS

In this paper, a novel family of Buck mode three-level direct ac converters with a high frequency link is proposed. The converters can transfer unsteady high ac voltage with distortion into regulated sinusoidal voltage with a low THD at the same frequency. The circuit configuration is constituted of a three-level converter, high frequency transformer, cycloconverter, and input and output filters. The topological

family includes the forward mode, interleaving forward mode, push-pull full-wave mode, push-pull full-bridge mode, half-bridge full-wave mode, half-bridge full-bridge mode, full-bridge full-wave mode and full-bridge full-bridge mode. By introducing a phase-shifted control strategy with the commutation overlap of the cycloconverter, the three-level ac-ac conversion and lower voltage stress of the power switches can be reliably achieved. In addition, the surge voltage and surge current of the cycloconverter are overcome.

This paper also describes the design and development of a prototype of a 500VA 220V±10% 50Hz ac/110V 50Hz ac converter. Experimental results are provided to show that the converters can reduce the voltage stress of the power switches, so that it is only half that of traditional two-level ac converters. The obtained experimental results also show that the input power factor is more than 0.670~0.9998 at the normalized capacity. This is much better than ac-dc-ac type TL ac converters that have an input power factor of 0.6~0.7. Furthermore, the low THD of the output voltage, the function of the bi-directional power flow and high frequency electrical isolation are also demonstrated in this paper.

ACKNOWLEDGMENT

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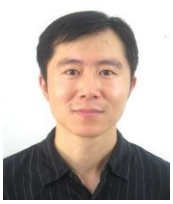

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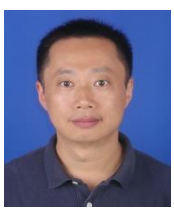

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